REMARKS

A. Background

The present amendment is filed in response to the Examiner's Office Action mailed May 16, 2003. Claims 1-31 were pending. Claims 11-21 and 26-31 were previously withdrawn from consideration. Claims 1 and 22 are amended. New claims 32-34 are added. Claims 1-10, 22-25, and 32-34 are now pending in view of the above amendments.

Reconsideration is respectfully requested in view of the above amendments and following remarks. For the Examiner's convenience and reference, Applicant's remarks are presented in the order in which the corresponding issues were raised in the Office Action.

B. Rejections Under 35 U.S.C. § 102

The Examiner rejects claims 1, 6, 22, 23, and 25 under 35 U.S.C. § 102 (b), as being anticipated by United States Patent No. 5,300,799 to Nakamura, *et al.* ("*Nakamura*"). As will be shown below, however, *Nakamura* -- assuming *arguendo* that it qualifies as a reference under Section 102 -- fails to teach or suggest each and every element of the pending claims, and thus does not anticipate the present claimed invention.

Nakamura discloses a non-volatile memory device utilizing ferroelectric capacitors. In particular, the device of *Nakamura* includes a plurality of source/drain diffusion regions 5 that cooperate during operation of the device to selectively program one or more ferroelectric capacitors FC1-FC8, as shown in Figure 1. In particular, *Nakamura* shows in Figure 1 that each of the source/drain regions 5 are equally disposed between corresponding ferroelectric capacitors FC1-FC8.

The claimed invention is substantially different than the device taught by *Nakamura*. Specifically, independent claim 1 requires the presence of a single transistor ferroelectric

memory cell including a semiconductor substrate having a source, a drain and a channel region, a gate oxide covering the source, drain, and channel region, and "a ferroelectric gate unit positioned on said gate oxide layer such that the ferroelectric gate unit overlies a relatively greater portion of the drain than the source." *Nakamura* teaches no such structure. Instead, as described above, *Nakamura* equally positions the source/drain diffusion regions between the ferroelectric capacitors FC1-FC8 (*see Nakamura* Figure 1), thereby causing each ferroelectric capacitor to overlie substantially equal portions of the respective source/drain diffusion regions. Accordingly, Applicant submits that *Nakamura* fails to teach or suggest each and every element of amended independent claim 1, and therefore fails to anticipate claim 1. Thus, claim 1 is allowable, and Applicant respectfully requests that the rejection of the claim under Section 102 be removed. Moreover, inasmuch as claims 2-10 are dependent on independent claim 1, Applicant submits that these claims are also allowable for at least the reasons given above. Allowance of these claims is therefore respectfully requested.

Amended independent claim 22 is patentably distinct for at least the same reasons set forth above. In particular, claim 22 requires, in a ferroelectric memory cell having a drain, source, channel covered by a gate oxide, the presence of a ferroelectric gate unit being positioned on the gate oxide," wherein the ferroelectric gate unit substantially overlies the entirety of the drain, and wherein the ferroelectric gate unit overlies only a portion of the source." Again, this limitation is not found in *Nakamura*. Thus, claim 22, as well as claims 23-25 that depend therefrom, are also allowable. Removal of the rejection under Section 102 and allowance of these claims is therefore respectfully requested.

C. **Rejections Under 35 U.S.C. § 103**

The Examiner rejects claims 2 and 24 under 35 U.S.C. § 103(a) as being unpatentable over *Nakamura* in view of United States Patent No. 5,506,748 to Hoshiba. The Examiner also rejects claim 3 under Section 103(a) as being unpatentable in view of *Nakamura* in view of United States Patent No. 6,100,558 to Krivokapic, *et al.* Further, the Examiner rejects claims 4, 7, and 8 under Section 103(a) as being unpatentable over *Nakamura*, and also rejects claim 5 under Section 103(a) as being unpatentable over *Nakamura* in view of a 1988 publication by Richard C. Jaeger. Finally, the Examiner rejects claim 9 under Section 103(a) as being unpatentable over *Nakamura* in view of United States Patent No. 6,339,008 to Takenaka and also rejects claim 10 as being unpatentable over *Nakamura* in view of United States Patent No. 6,172,392 to Schmidt, *et al.*

Applicant notes that each of the above rejections is at least partly based on the *Nakamura* reference. Applicant further notes that each of the rejected claims as set forth above is dependent upon either amended independent claim 1 or 22. As was previously discussed, the teachings of *Nakamura* are inapplicable to the present invention as applied to claims 1 and 22 for failing to teach or suggest each of the limitations contained in those claims. Thus, *Nakamura* is equally inapplicable to the present claims rejected under Section 103 for at least the above reasons, that is, its failure to teach or suggest all of the claim limitations contained not only in independent claims 1 or 22, but also the limitations contained in the presently rejected dependent claims. Thus, the Office Action has failed to establish a *prima facie* case of obviousness. Applicant therefore respectfully submits that claims 2-5, 7, 8-10, and 24 are allowable and that the above rejection under Section 103 should be withdrawn.

D. New Claims

Applicant submits that new claims 32-34 are also allowable in light of the cited references. In particular, new independent claim 33 discloses a ferroelectric memory cell that includes a ferroelectric gate unit positioned on a gate oxide layer covering a drain, source, and channel, "the ferroelectric gate unit asymmetrically overlying the drain with respect to the source." Because, as discussed above, *Nakamura* fails to teach any such device, Applicant respectfully submits that claim 33 and its dependent claim 34 are allowable. In addition, claim 32 is dependent upon independent claim 1, which is allowable for at least the reasons already stated above. Thus, claim 32 is also allowable.

E. Amendment to the Specification

Applicant has amended the specification to clarify selected aspects of one embodiment of the present invention, shown in Figures 5 and 6. In particular, a new paragraph has been added to clarify certain positional relationships between the FEM gate unit 32, the source 16, and the drain 18 of each FEM cell 50 shown in Figures 5 and 6. Applicant submits that no new matter has been added as a result of this amendment to the specification. Indeed, the positional relationships described in the new paragraph are clearly shown in Figures 5 and 6, which remain unchanged and which were present in the application as originally filed. Further support for the new paragraph can also be found in the paragraph beginning at line 16 on page 4, the paragraph beginning at line 9 on page 9, the paragraph beginning at line 7 on page 10, and the paragraph beginning at line 21 on page 12 in the specification as originally filed. Entry of this amendment is respectfully solicited.

CONCLUSION

In view of the discussion and amendments submitted herein, Applicant respectfully submits that each of the pending claims 1-10, 22-25, and 32-34 is now in condition for allowance. Therefore, reconsideration of the rejections is requested and allowance of those claims is respectfully solicited. In the event that the Examiner finds any remaining impediment to a prompt allowance of this application that can be clarified in a telephonic interview, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 30th day of April, 2004.

Respectfully submitted,

Kevin W. Stinger
Attorney for Applicant
Registration No. 48,959
Customer No. 022913

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